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**IBM Power5 chip: a dual-core multithreaded processor - all 17 versions »**

R Kalla, B Sinharoy, JM Tandler - Micro, IEEE, 2004 - [ieeexplore.ieee.org](#)

... the Power5 was to maintain both binary and structural **compatibility** with existing ...

In the Power5, two groups can commit **per cycle**, one from each **thread**. ...

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**[PDF] MAJC (tm): An Architecture for the New Millennium - all 3 versions »**

M Tremblay - Proc. Hot Chips, 1999 - [dlhoffman.com](#)

... I hits run in 1 **cycle**: 95 cycles ... I Each group can be "enabled" for each **thread** ... Sun

Microsystems/MT 27 Conclusion I Not having binary **compatibility** (legacy) ...

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**Microprocessors circa 2000 - all 3 versions »**

PP Gelsinger, PA Gargini, GH Parker, AYC Yu - Spectrum, IEEE, 1989 - [ieeexplore.ieee.org](#)

... If this is so, general-purpose **compatible** computing families ... **per- instruction** barrier

in the **near** future. ... The concept of **threads** (an in- dependently executable ...

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**Multithreaded processor architectures - all 4 versions »**

GT Byrd, MA Holliday - Spectrum, IEEE, 1995 - [ieeexplore.ieee.org](#)

... ned Sparc:e. Star T-f4G) Fine-grained (HEP, Tera MTr, Laudcrl jij A Multithreading

systems that Issue **instructions** from only one **thread per cycle** are either ...

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**Relational profiling: enabling thread-level parallelism in virtualmachines - all 7 versions »**

T Heil, JE Smith - Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual ..., 2000 - [ieeexplore.ieee.org](#)

... information collected to seven words **per record**. ... Information **Instruction PC Thread**

ID Input operand values ... Exceptions and branch outcome **Cycle** when **instruction** ...

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**Evolving Mach 3.0 to a migrating thread model - all 6 versions »**

B Ford, J Lepreau - Usenix Winter Conference, CA, 1994 - [usenix.org](#)

... operating systems support multiple **threads per process (per** ... We maintain

**compatibility**

with existing Mach code by ... ports direct replacements for **thread** ports at ...

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**Billion-Transistor Architectures - all 7 versions »**

D Burger, JR Goodman - Computer, 1997 - [ieeexplore.ieee.org](#)

... have significant similarities: each maintains **compatibility** with old ... par- allelism

can compensate for a lack of **per-thread** ... see SMT processors in the **near** future ...

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**The MAJC Architecture: A Synthesis of Parallelism and Scalability - all 15 versions »**

**A Portable Programming Interface for Performance Evaluation on Modern Processors - all 15 versions »**

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**Introduction to the Cell multiprocessor - all 7 versions »**

J Kahle... - IBM Journal of Research and Development, 2005 - research.ibm.com

 ... In addition, **compatibility** with the Power Architecture ... 128-bit vector register file **per thread**, and all ... yet several applications achieve **near-peak** performance ...

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**Montecito: a dual-core, dual-thread Itanium processor - all 11 versions »**

C McNairy, R Bhatia - Micro, IEEE, 2005 - ieeexplore.ieee.org

 ... optimization **compatibility**—which lets proces- sors run each ... using all the available cache, **thread**, and core ... technology can provide a **near** cubic reduction in ...

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**Hardware-software interactions on Mpact - all 5 versions »**

P Kalapathy, CR Inc, CA Sunnyvale - Micro, IEEE, 1997 - ieeexplore.ieee.org

 ... MRK schedules all **threads** to be run on Mpact using a ... The Mpact chip is **compatible** with standard PC-AT lega- cy ... The dividing line **near** the bottom of the figure ...

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**[PDF] Compatible phase co-scheduling on a CMP of multi-threaded processors - all 4 versions »**

A El-Moursy, R Garg, DH Albonesi, S Dwarkadas - Intl. Parallel and Distributed Processing Symp, 2006 - ece.rochester.edu

 ... core chips, the most prominent **near-** term use ... we run for one 100K **cycle** interval before ... functional unit (FU) contention on **thread compatibility**, we performed ...

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**Compiler optimization of scalar value communication between speculative threads - all 19 versions »**

A Zhai, CB Colohan, JG Steffan, TC Mowry - ACM SIGPLAN Notices, 2002 - portal.acm.org

 ... data, 2 for insts Crossbar Interconnect 8B **per cycle per bank** Minimum ... Main Memory Bandwidth 1 access **per 20 cycles** ... latency nor the cost of **thread** creation into ...

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**A high speed dataflow processing element and its performance compared to a von Neumann mainframe**

JN Coleman - Parallel Processing Symposium, 1993., Proceedings of Seventh ..., 1993 - ieeexplore.ieee.org

 ... reduces the exhibition of locality, although when many **threads** are executing the ... 7-fold parallelism to maintain an execution rate of one **cycle per instruction**. ...

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**Next Generation Embedded Processor Architecture for Personal Information Devices**

I Hong, Y Lee, Y Lee - LECTURE NOTES IN COMPUTER SCIENCE, 2006 - Springer

 ... loader and system call handling routine that is **compatible** with ARM ... architecture, a maximum of four **instructions** from a **thread** can be issued every **cycle**. ...

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**System and method for CPI load balancing in SMT processors**

JM Accapadi, A Dunshea, D Michel, MS Srinivas - 2005 - freepatentsonline.com

... method that uses a measurement to determine processing **threads** that are **compatible** with one ... average number of operations executed **per clock cycle** is to ...[Cached](#) - [Web Search](#)**Converting a processor into a compatible virtual multithreaded processor (VMP)**

G Vinitzky, E Dagan - 2007 - freepatentsonline.com

... phases, the new multithreaded processor is not **compatible** with the ... The total throughputof pipeline 200, executing 4 **threads**, is 1 **instruction per cycle**. ...[Cached](#) - [Web Search](#)**System and method for CPI scheduling on SMT processors**

JM Accapadi, A Dunshea, D Michel, MS Srinivas - 2005 - freepatentsonline.com

... method that uses a measurement to determine processing **threads** that are **compatible** with one ... average number of operations executed **per clock cycle** is to ...[Cached](#) - [Web Search](#)Result Page: [Previous](#) [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [11](#) [Next](#) [Google Home](#) - [About Google](#) - [About Google Scholar](#)

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